WHAT IS CLAIMED IS:

1. A digital dynamic convergence error control system, comprising:

a convergence error detecting apparatus recognizing crossing points of a screen pattern displayed on a screen of a display device, detecting each amount of convergence errors corresponding to respective crossing points;

a main control means generating correction data in response to respective convergence errors, generating interpolation data using said correction data of adjacent crossing points; and

a digital dynamic convergence error control apparatus receiving said correction data and said interpolation data from said main control means, storing said correction data and said interpolation data in a memory, converting each of said correction data and said interpolation data into voltage or current in response to respective horizontal synchronization signals extracted from a picture signal, and independently and separately applying said voltage or said current to a magnetic field controlling coil only during a corresponding period of respective horizontal synchronization signals.

2. The system of claim 1, said digital dynamic convergence error control apparatus being integrated in a single chip having a monolithic structure.

3. The system of claim 1, said crossing points of said screen pattern corresponding to respective correction data and being formed by horizontal lines and vertical lines.

4. The system of claim 1, said interpolation data generated in an area disposed between said adjacent crossing points of said screen pattern, said area corresponding to horizontal synchronization signals of said picture signal disposed between said adjacent crossing points of said screen pattern, said crossing points of said screen pattern being formed by horizontal lines and vertical lines.

5. The system of claim 1, said digital dynamic convergence error control apparatus comprising:

a controller receiving said correction data, said interpolation data, and control command signals from said main control means, generating address corresponding to each of said correction data and said interpolation data, storing said correction data and said interpolation data in respective addresses of said memory, controlling an address bus and a data bus to read said correction data and said interpolation data from respective addresses of said memory;

a reference clock generator generating clock signals in response to a clock control signal inputted from said controller;

an address generator generating an interrupt signal and setup signals for calculating said interpolation data corresponding to an area between adjacent crossing points in response to horizontal and vertical synchronization signals extracted from said picture signal, control signals generated from said controller, and said clock signals generated from said reference clock generator;

an internal memory storing said correction data and said interpolation data inputted into said controller; and

an output section converting said correction data and said interpolation data into said voltage and said current in response to output control signals generated from said controller and a conversion control signal generated from said address generator, and applying said voltage and said current to said magnetic field controlling coils for generating more than two pole magnetic fields.

6. The system of claim 5, said control signals of said controller including a skip number, a first dividing ratio, a pass number, and a second dividing ratio, a first comparator clock number, and a main clock signal transmitted to said reference clock generator.

7. The system of claim 5, said setup signals of said controller including an NCNT signal, a horizontal address, a vertical address, a horizontal control signal, and a vertical control signal.

8. The system of claim 5, further comprising a nonvolatile external memory disposed outside said digital dynamic convergence error correction apparatus, coupled to said controller, storing said correction data and said interpolation data, said correction data and said interpolation data stored in said nonvolatile memory transmitted to said internal memory in response to a request signal of said controller.

9. The system of claim 5, said digital dynamic convergence error control apparatus comprising said controller generating said control signals by counting the number of said clock signals generated from said reference clock generator during a period of a horizontal synchronization signal of said picture signal in response to said clock control signal of said controller, said address generator of digital dynamic convergence error control apparatus comprising:

a first counter and a first comparator generating an NCNT signal as one of setup signals in response to said number of said clock signals counted during said period of said horizontal synchronization signal, generating a first interrupt signal whenever there exists a difference between the NCNT and a reference;

a first divider receiving a skip number and a first dividing ratio, generating a horizontal control signal as one of said setup signals after dividing by said first dividing ratio a remaining portion of said horizontal synchronization signal remained after skipping said horizontal synchronization signal by a number of clock signals corresponding to the skip number;

a second counter generating horizontal address signal by counting the horizontal control signal generated from said first divider;

a second divider receiving a pass number and a second dividing ratio and generating a vertical control signal after dividing by said second dividing ratio a remaining portion of said

vertical synchronization signal remained after passing a number of horizontal synchronization signals corresponding to the pass number during said vertical synchronization signal;

a third counter generating a vertical address signal by counting the vertical control signal generated from said second divider;

a fourth counter generating a count value by counting the number of clocks of the horizontal synchronization signal during a vertical synchronization signal period; and

a second comparator receiving said count value generated from fourth counter, outputting a second interrupt signal whenever a difference between the count value and a second reference by counting the number of clocks in every vertical synchronization signal only when said first comparator generates said first interrupt signal.

10. The system of claim 5, said digital dynamic convergence error control apparatus comprising:

a plurality of digital to analog converters converting into each analog signal said correction data and said interpolation data corresponding to respective magnetic field correcting coils generating more than two pole magnetic fields corresponding to respective vertical and horizontal axes of said magnetic field correcting coils; and

a plurality of correction and interpolation units coupled to respective said digital to analog converters, receiving said correction data and said interpolation data from said internal memory, transmitting said correction data and said interpolation data to corresponding digital to analog converter so as to control respective magnetic field controlling coils designated by each coil address generated from said address generator with corresponding correction data and corresponding interpolation data.

11. The system of claim 5, said digital dynamic convergence error control apparatus comprising:

a first memory storing and outputting said correction data in response to said horizontal and vertical address;

a second memory storing and outputting the interpolation data in response to said horizontal and vertical address;

a counter for receiving vertical and horizontal synchronization signals from said address generator and each line number of said interpolation data from said second memory, counting each line number of said horizontal synchronization signals existing during the vertical control signal by skipping said line number of said horizontal synchronization signals corresponding to said interpolation data;

a multiplier for outputting a multiplied output signal by multiplying a counted signal of said counter with said interpolation data transmitted from said second controller in response to an enable signal generated in accordance with said line number of said interpolation data from said second memory;

a code bit discriminator for receiving and recognizing said interpolation data from said second memory, outputting an operation signal depending on the status of said interpolation data; and

an adder and a subtracter for receiving said correction data from said first memory and said interpolation data from said second memory, adding and subtracting said multiplied output signal of said multiplier in response to said operation signal from said code bit discriminator.

12. A digital dynamic convergence error control apparatus, comprising:

a nonvolatile external memory storing correction data and interpolation data for correcting convergence errors corresponding to crossing points of a screen pattern;

a controller receiving said correction data and said interpolation data from said nonvolatile external memory through a data bus and an address bus, generating control signals for proceeding a convergence error correcting and interpolating process for each portion of said screen pattern;

a reference clock generator generating clock signals in response to a clock control signal inputted from said controller;

an address generator generating an interrupt signal and setup signals for calculating said interpolation data corresponding to an area between adjacent crossing points in response to horizontal and vertical synchronization signals extracted from said picture signal, control signals generated from said controller, and said clock signals generated from said reference clock generator;

an internal memory storing said correction data and said interpolation data inputted into said controller; and

an output section converting said correction data and said interpolation data into said voltage and said current in response to output control signals generated from said controller and a conversion control signal generated from said address generator, and applying said voltage and said current to said magnetic field controlling coils for generating more than two pole magnetic fields.

13. The apparatus of claim 12, said digital dynamic convergence error control apparatus being made of a single semiconductor chip in a monolithic structure excluding said nonvolatile external memory.

14. The apparatus of claim 12, said crossing points of said screen pattern corresponding to respective correction data and being formed by horizontal lines and vertical lines.

15. The apparatus of claim 12, said interpolation data generated in an area disposed between said adjacent crossing points of said screen pattern, said area corresponding to horizontal synchronization signals of said picture signal disposed between said adjacent crossing points of said screen pattern, said crossing points of said screen pattern being formed by horizontal lines and vertical lines.

16. The apparatus of claim 12, said control signals of said controller including a

skip number, a first dividing ratio, a pass number, and a second dividing ratio, a first comparator clock number, and a main clock signal transmitted to said reference clock generator.

17. The apparatus of claim 12, said setup signals of said address generator including an NCNT signal, a horizontal address, a vertical address, a horizontal control signal, and a vertical control signal.

18. The apparatus of claim 12, said controller generating said control signals by counting the number of said clock signals generated from said reference clock generator during a period of a horizontal synchronization signal of said picture signal in response to said clock control signal of said controller, said address generator of said digital dynamic convergence error control apparatus comprising:

a first counter and a first comparator generating an NCNT signal as one of setup signals in response to said number of said clock signals counted during said period of said horizontal synchronization signal, generating a first interrupt signal whenever there exists a difference between the NCNT and a reference;

a first divider receiving a skip number and a first dividing ratio, generating a horizontal control signal as one of said setup signals after dividing by said first dividing ratio a remaining portion of said horizontal synchronization signal remained after skipping said horizontal synchronization signal by a number of clock signals corresponding to the skip number;

a second counter generating horizontal address signal by counting the horizontal control signal generated from said first divider;

a second divider receiving a pass number and a second dividing ratio and generating a vertical control signal after dividing by said second dividing ratio a remaining portion of said vertical synchronization signal remained after passing a number of horizontal synchronization signals corresponding to the pass number during said vertical synchronization signal;

a third counter generating a vertical address signal by counting the vertical control signal generated from said second divider;

a fourth counter generating a count value by counting the number of clocks of the horizontal synchronization signal during a vertical synchronization signal period; and

a second comparator receiving said count value generated from fourth counter, outputting a second interrupt signal whenever a difference between the count value and a second reference by counting the number of clocks in every vertical synchronization signal only when said first comparator generates said first interrupt signal.

19. The apparatus of claim 12, said output section comprising:

a plurality of digital to analog converters converting into each analog signal said correction data and said interpolation data corresponding to respective magnetic field correcting coils generating more than two pole magnetic fields corresponding to respective vertical and horizontal axes of said magnetic field correcting coils; and

a plurality of correction and interpolation sections coupled to respective said digital to analog converters, receiving said correction data and said interpolation data from said internal memory, transmitting said correction data and said interpolation data to corresponding digital to analog converter so as to control respective magnetic field controlling coils designated by each coil address generated from said address generator with corresponding correction data and said interpolation data.

20. The apparatus of claim 12, further comprising a correction and interpolation section including:

a first memory storing and outputting the correction data in response to said horizontal and vertical addresses;

a second memory storing and outputting the interpolation data in response to said horizontal and vertical address;

a counter for receiving vertical and horizontal synchronization signals from said address generator and each line number of said interpolation data from said second memory, counting each line number of said horizontal synchronization signals existing during the vertical control signal by skipping said line number of said horizontal synchronization signals

corresponding to said interpolation data;

a multiplier for outputting a multiplied output signal by multiplying a counted signal of said counter with said interpolation data transmitted from said second controller in response to an enable signal generated in accordance with said line number of said interpolation data from said second memory;

a code bit discriminator for receiving and recognizing said interpolation data from said second memory, outputting an operation signal depending on the status of said interpolation data; and

an adder and a subtracter for receiving said correction data from said first memory and said interpolation data from said second memory, adding and subtracting said multiplied output signal of said multiplier in response to said operation signal from said code bit discriminator.

21. A deflection yoke having a digital dynamic convergence error correcting apparatus, comprising:

a coil separator having a neck portion coupled to a CRT;

a horizontal deflection coil and a vertical deflection coil provided on said coil separator;

a plurality of magnetic field controlling coils for generating more than two pole magnetic fields;

a nonvolatile external memory storing correction data and interpolation data for correcting convergence errors corresponding to crossing points of a screen pattern;

a controller receiving said correction data and said interpolation data from said nonvolatile external memory through a data bus and an address bus, generating control signals for proceeding a convergence error correcting and interpolating process for each portion of said screen pattern;

a reference clock generator generating clock signals in response to a clock control signal inputted from said controller;

an address generator generating an interrupt signal and setup signals for calculating said interpolation data corresponding to an area between adjacent crossing points in response to horizontal and vertical synchronization signals extracted from said picture signal, control signals generated from said controller, and said clock signals generated from said reference clock generator;

an internal memory storing said correction data and said interpolation data inputted into said controller; and

an output section converting said correction data and said interpolation data into said voltage and said current in response to output control signals generated from said controller and a conversion

control signal generated from said address generator, and applying said voltage and said current to said magnetic field controlling coils for generating more than two pole magnetic fields.

22. The deflection yoke of claim 21, wherein said controller, said reference clock generator, said address generator, said internal memory, and said output section all being integrated in a single semiconductor chip having a monolithic structure.

23. The deflection yoke of claim 21, said crossing points of said screen pattern corresponding to respective correction data and being formed by horizontal lines and vertical lines.

24. The deflection yoke of claim 21, said interpolation data generated in an area disposed between said adjacent crossing points of said screen pattern, said area corresponding to horizontal synchronization signals of said picture signal disposed between said adjacent crossing points of said screen pattern, said crossing points of said screen pattern being formed by horizontal lines and vertical lines.

25. The deflection yoke of claim 21, said control signals of said controller including a skip number, a first dividing ratio, a pass number, and a second dividing ratio, a first comparator clock number, and a main clock signal transmitted to said reference clock generator.

26. The deflection yoke of claim 21, said setup signals of said address generator including an NCNT signal, a horizontal address, a vertical address, a horizontal control signal, and a vertical control signal.

27. The deflection yoke of claim 21, said controller generating said control signals by counting the number of said clock signals generated from said reference clock generator during a period of a horizontal synchronization signal of said picture signal in response to said clock control signal of said controller, said address generator of said digital dynamic convergence error control apparatus comprising:

a first counter and a first comparator generating an NCNT signal as one of setup signals in response to said number of said clock signals counted during said period of said horizontal synchronization signal, generating a first interrupt signal whenever there exists a difference between the NCNT and a reference;

a first divider receiving a skip number and a first dividing ratio, generating a horizontal control signal as one of said setup signals after dividing by said first dividing ratio a remaining portion of said horizontal synchronization signal remained after skipping said horizontal synchronization signal by a number of clock signals corresponding to the skip number;

a second counter generating horizontal address signal by counting the horizontal control signal generated from said first divider;

a second divider receiving a pass number and a second dividing ratio and generating a vertical control signal after dividing by said second dividing ratio a remaining portion of said vertical synchronization signal remained after passing a number of horizontal synchronization signals corresponding to the pass number during said vertical synchronization signal;

a third counter generating a vertical address signal by counting the vertical control signal generated from said second divider;

a fourth counter generating a count value by counting the number of clocks of the horizontal synchronization signal during a vertical synchronization signal period; and

a second comparator receiving said count value generated from fourth counter, outputting a second interrupt signal whenever a difference between the count value and a second reference by counting the number of clocks in every vertical synchronization signal only when said first comparator generates said first interrupt signal.

28. The deflection yoke of claim 21, said output section comprising:

a plurality of digital to analog converters converting into each analog signal said correction data and said interpolation data corresponding to respective magnetic field correcting coils generating more than two pole magnetic fields corresponding to respective vertical and horizontal axes of said magnetic field correcting coils; and

a plurality of correction and interpolation sections coupled to respective said digital to analog converters, receiving said correction data and said interpolation data from said internal memory, transmitting said correction data and said interpolation data to corresponding digital to analog converter so as to control respective magnetic field controlling coils designated by each coil address generated from said address generator with corresponding correction data and said interpolation data.

29. The deflection yoke of claim 21, further comprising a correction and interpolation section including:

a first memory storing and outputting the correction data in response to said horizontal and vertical address;

a second memory storing and outputting the interpolation data in response to said horizontal and vertical address;

a counter for receiving vertical and horizontal synchronization signals from said

address generator and each line number of said interpolation data from said second memory, counting each line number of said horizontal synchronization signals existing during the vertical control signal by skipping said line number of said horizontal synchronization signals corresponding to said interpolation data;

a multiplier for outputting a multiplied output signal by multiplying a counted signal of said counter with said interpolation data transmitted from said second controller in response to an enable signal generated in accordance with said line number of said interpolation data from said second memory;

a code bit discriminator for receiving and recognizing said interpolation data from said second memory, outputting an operation signal depending on the status of said interpolation data; and

an adder and a subtracter for receiving said correction data from said first memory and said interpolation data from said second memory, adding and subtracting said multiplied output signal of said multiplier in response to said operation signal from said code bit discriminator.

30. A display device having a digital dynamic convergence error correcting apparatus, comprising:

a deflection yoke deflecting electron beams emitted from an electron gun of a CRT;

a plurality of magnetic field controlling coils for generating more than two pole magnetic fields;

a nonvolatile external memory storing correction data and interpolation data for correcting convergence errors corresponding to crossing points of a screen pattern;

a controller receiving said correction data and said interpolation data from said nonvolatile external memory through a data bus and an address bus, generating control signals for proceeding a convergence error correcting and interpolating process for each portion of said screen pattern;

a reference clock generator generating clock signals in response to a clock control

signal inputted from said controller;

an address generator generating an interrupt signal and setup signals for calculating said interpolation data corresponding to an area between adjacent crossing points in response to horizontal and vertical synchronization signals extracted from said picture signal, control signals generated from said controller, and said clock signals generated from said reference clock generator;

an internal memory storing said correction data and said interpolation data inputted into said controller; and

an output section converting said correction data and said interpolation data into said voltage and said current in response to output control signals generated from said controller and a conversion

control signal generated from said address generator, and applying said voltage and said current to said magnetic field controlling coils for generating more than two pole magnetic fields.

31. The display device of claim 30, wherein said controller, said reference clock generator, said address generator, said internal memory, and said output section all being integrated in a single semiconductor chip having a monolithic structure.

32. The display device of claim 30, said crossing points of said screen pattern corresponding to respective correction data and being formed by horizontal lines and vertical lines.

33. The display device of claim 30, said interpolation data generated in an area disposed between said adjacent crossing points of said screen pattern, said area corresponding to horizontal synchronization signals of said picture signal disposed between said adjacent crossing points of said screen pattern, said crossing points of said screen pattern being formed by horizontal lines and vertical lines. said convergence error correction data being

corresponding to respective crossing points of said screen pattern being formed by horizontal lines and vertical lines.

34. The display device of claim 30, said control signals of said controller including a skip number, a first dividing ratio, a pass number, and a second dividing ratio, a first comparator clock number, and a main clock signal transmitted to said reference clock generator.

35. The display device of claim 30, said setup signals of said address generator including an NCNT signal, a horizontal address, a vertical address, a horizontal control signal, and a vertical control signal.

36. The display device of claim 30, said controller generating said control signals by counting the number of said clock signals generated from said reference clock generator during a period of a horizontal synchronization signal of said picture signal in response to said clock control signal of said controller, said address generator of digital dynamic convergence error control apparatus comprising:

a first counter and a first comparator generating an NCNT signal as one of setup signals in response to said number of said clock signals counted during said period of said horizontal synchronization signal, generating a first interrupt signal whenever there exists a difference between the NCNT and a reference;

a first divider receiving a skip number and a first dividing ratio, generating a horizontal control signal as one of said setup signals after dividing by said first dividing ratio a remaining portion of said horizontal synchronization signal remained after skipping said horizontal synchronization signal by a number of clock signals corresponding to the skip number;

a second counter generating horizontal address signal by counting the horizontal control signal generated from said first divider;

a second divider receiving a pass number and a second dividing ratio and generating a

vertical control signal after dividing by said second dividing ratio a remaining portion of said vertical synchronization signal remained after passing a number of horizontal synchronization signals corresponding to the pass number during said vertical synchronization signal;

a third counter generating a vertical address signal by counting the vertical control signal generated from said second divider;

a fourth counter generating a count value by counting the number of clocks of the horizontal synchronization signal during a vertical synchronization signal period; and

a second comparator receiving said count value generated from fourth counter, outputting a second interrupt signal whenever a difference between the count value and a second reference by counting the number of clocks in every vertical synchronization signal only when said first comparator generates said first interrupt signal.

37. The display device of claim 30, said output section comprising:

a plurality of digital to analog converters converting into each analog signal said correction data and said interpolation data corresponding to respective magnetic field correcting coils generating more than two pole magnetic fields corresponding to respective vertical and horizontal axes of said magnetic field correcting coils; and

a plurality of correction and interpolation sections coupled to respective said digital to analog converters, receiving said correction data and said interpolation data from said internal memory, transmitting said correction data and said interpolation data to corresponding digital to analog converter so as to control respective magnetic field controlling coils designated by each coil address generated from said address generator with corresponding correction data and said interpolation data.

38. The display device of claim 30, further comprising a correction and interpolation section including:

a first memory storing and outputting the correction data in response to said horizontal and vertical address;

a second memory storing and outputting the interpolation data in response to said horizontal and vertical address;

a counter for receiving vertical and horizontal synchronization signals from said address generator and each line number of said interpolation data from said second memory, counting each line number of said horizontal synchronization signals existing during the vertical control signal by skipping said line number of said horizontal synchronization signals corresponding to said interpolation data;

a multiplier for outputting a multiplied output signal by multiplying a counted signal of said counter with said interpolation data transmitted from said second controller in response to an enable signal generated in accordance with said line number of said interpolation data from said second memory;

a code bit discriminator for receiving and recognizing said interpolation data from said second memory, outputting an operation signal depending on the status of said interpolation data; and

an adder and a subtracter for receiving said correction data from said first memory and said interpolation data from said second memory, adding and subtracting said multiplied output signal of said multiplier in response to said operation signal from said code bit discriminator.

39. An apparatus for generating a convergence reference signal for correcting convergence errors in a picture displayed on a screen of a CRT by controlling a plurality of magnetic field controlling coils for generating more than two pole magnetic fields corresponding to one of horizontal and vertical axes, comprising:

a controller generating control signals including a skip number, a pass number, a first dividing ratio, a second dividing ratio, and clocks;

a first counter and a first comparator generating a counted number by counting the number of said clocks during a period of a horizontal synchronization signal, generating a first interrupt signal whenever there exists a difference between said counted number and a

reference number;

a first divider receiving said skip number and said first dividing ratio, subtracting said the number of said clocks corresponding to the skip number from the period of the horizontal synchronization signal, dividing a remaining period of the subtracted horizontal synchronization signal by the first dividing ratio, and generating a horizontal control signal.

a second counter generating a horizontal address signal by counting said horizontal control signal generated from said first divider;

a second divider receiving said second dividing ratio and said pass number representing that a number of horizontal synchronization signals are eliminated, subtracting the number of horizontal synchronization signals corresponding to the pass number from a total number of horizontal synchronization signals during a period of said vertical synchronization signal, dividing a remaining number of said horizontal synchronization signals of said vertical synchronization signal by said second dividing ratio, and generating a vertical control signal;

a third counter generating a vertical address signal by counting said vertical control signal;

a fourth counter generating a count value by counting the number of clocks of the horizontal synchronization signal during a vertical synchronization signal period; and

a second comparator receiving the count value generated from said fourth counter and outputting a second interrupt signal whenever a difference between the count value and a reference value in every vertical synchronization signal only when said first comparator generates said first interrupt signal.

40. The apparatus of claim 39, wherein said convergence reference signal for correcting convergence errors in a picture displayed on a screen of a CRT is generated in response to said control signals by reading correction data and interpolation data stored in a memory coupled to said apparatus in accordance with the number of said clocks counted during said period of said horizontal synchronization signal.

41. A correcting and interpolating apparatus in a digital dynamic convergence error correcting apparatus, comprising:

an address generator for generating a convergence error correction reference point address for correcting convergence errors of a picture displayed in a screen of a CRT;

an interpolating apparatus for performing a convergence error correcting and interpolating process by controlling respective magnetic field controlling coils corresponding to vertical and horizontal axes;

a first memory storing and outputting the correction data in response to said horizontal and vertical address;

a second memory storing and outputting the interpolation data in response to said horizontal and vertical address;

a counter for receiving vertical and horizontal synchronization signals from said address generator and each line number of said interpolation data from said second memory, counting each line number of said horizontal synchronization signals existing during the vertical control signal by skipping said line number of said horizontal synchronization signals corresponding to said interpolation data;

a multiplier for outputting a multiplied output signal by multiplying a counted signal of said counter with said interpolation data transmitted from said second controller in response to an enable signal generated in accordance with said line number of said interpolation data from said second memory;

a code bit discriminator for receiving and recognizing said interpolation data from said second memory, outputting an operation signal depending on the status of said interpolation data; and

an adder and a subtracter for receiving said correction data from said first memory and said interpolation data from said second memory, adding and subtracting said multiplied output signal of said multiplier in response to said operation signal from said code bit discriminator.

42. The interpolating apparatus of claim 41, wherein an area for correcting said convergence error in accordance with said correction data outputted from said first memory corresponds to respective correction points of said screen indicated by respective convergence error correction reference point addresses.

43. The display device of claim 41, wherein an area for being interpolated in accordance with said interpolation data outputted from said second memory corresponds to said horizontal synchronization signals disposed between correction points indicated by respective adjacent convergence error correction reference point addresses.

44. A convergence error correcting apparatus in a display device, comprising a memory storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within a period of a specific horizontal synchronization signal.

45. A convergence error correcting apparatus in a display device, comprising a memory storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within each period of specific horizontal synchronization signals, said memory storing a plurality of interpolation data signals corresponding to horizontal synchronization signals disposed between adjacent correction points.

46. A convergence error correcting apparatus in a display device, comprising a controller independently and separately generating a plurality of independent and separate convergence error correction data signals corresponding to respective correction points of a screen pattern and independently and separately applying each of convergence error correction data signals to magnetic field controlling coils when each correction point corresponding to

respective convergence error correction data signals is scanned in a screen.

47. A convergence error correcting apparatus in a display device, comprising:

a memory storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within each period of specific horizontal synchronization signals, said memory storing a plurality of interpolation data signals corresponding to horizontal synchronization signals disposed between adjacent correction points; and

a controller coupled to said memory, independently reading each of said convergence error correction data signals from said memory when corresponding correction point is scanned in a screen.

48. A convergence error correcting apparatus in a display device, comprising a controller generating a first separate and independent convergence error correction data corresponding to respective first pixels in a first screen having a first screen size in response to the number of first horizontal synchronization signals in a first vertical synchronization signal, said controller generating a first separate and independent interpolation data signals corresponding to a first area disposed between adjacent first pixels, said controller generating a second separate and independent convergence correction data corresponding to respective second pixels in a second screen having a second screen size in response to the number of second horizontal synchronization signals in a second vertical synchronization signal, said controller generating a second separate and independent interpolation data signals corresponding to a second area disposed between adjacent second pixels.

49. A process in a convergence error correcting apparatus, comprising the steps of:

storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within each period of specific horizontal

synchronization signals;

storing a plurality of interpolation data signals corresponding to horizontal synchronization signals disposed between adjacent correction points; and

independently and separately generating a plurality of independent and separate convergence error correction data signals corresponding to respective correction points of a screen pattern and independently and separately applying each of convergence error correction data signals to magnetic field controlling coils when each correction point corresponding to respective convergence error correction data signals is scanned in a screen.

50. A process in a convergence error correcting apparatus, comprising the steps of:

storing a first separate and independent convergence error correction data corresponding to respective first pixels in a first screen having a first screen size in response to the number of first horizontal synchronization signals in a first vertical synchronization signal;

storing a first separate and independent interpolation data signals corresponding to a first area disposed between adjacent first pixels;

converting said first convergence error correction data signals and said first interpolation data signals into a second separate and independent convergence correction data and a second interpolation data signals corresponding to respective second pixels in a second screen signal having a second screen size in response to the number of second horizontal synchronization signals in a second vertical synchronization signal.